A W-Band Source Module Using MMIC's

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Abstract—**A W-band source module providing 4-GHz tuning bandwidth (92.5–96.5 GHz) has been developed. This module consists of three MMIC chips: a 23.5 GHz HBT VCO, a 23.5–94 GHz HEMT frequency quadrupler and a W-band three-stage HEMT output amplifier, all fabricated in TRW production lines. It exhibits a measured output power of 3 dBm at 94–95 GHz and a 3-dB tuning bandwidth greater than 3 GHz, with a phase noise of −92 dBc/Hz at 1 MHz offset. This work demonstrates a new and efficient way to implement high performance W-band source. Its wide tuning bandwidth with good phase noise performance, as well as design simplicity, makes this approach attractive for many W-band system applications.**

I. Introduction

LOW PHASE noise and stable frequency sources are required in millimeter-wave (MMW) systems. These frequency sources can be generated by either fundamental frequency oscillators or using lower frequency oscillators in conjunction with frequency multipliers to obtain desired frequencies. Several MMW frequency sources have been reported using monolithic technology, including fundamental frequency oscillators at W-band (75–110 GHz) [1], [2], and lower frequency oscillators in conjunction with frequency multipliers at V-band (50–75 GHz) [3] as well as W-band [4]. There are advantages for the later approach. It is easier to achieve low phase noise for an oscillator operating at lower frequency. Also, a wider bandwidth can be achieved owing to frequency multiplication and reduced parasitics at lower frequency.

This paper reports a W-band source module using three MMIC chips: a 23.5 GHz heterojunction bipolar transistor (HBT) voltage control oscillator (VCO) driving a 23.5–94 GHz high electron mobility transistor (HEMT) frequency quadrupler and driving a W-band three-stage HEMT output amplifier. The W-band source module has a tuning bandwidth of 4 GHz from 92.5–96.5 GHz and exhibits a maximum output power of 3 dBm at 94–95 GHz and a 3-dB tuning bandwidth greater than 3 GHz, with a phase noise of −92 dBc/Hz at 1 MHz offset. This work demonstrates a new and efficient way to implement high performance W-band source. Its wide tuning bandwidth with good phase noise performance, as well as design simplicity, makes this approach attractive for many W-band system applications. In addition, all of the MMIC chips used in this module were fabricated at TRW GaAs MMIC production lines and therefore can be produced in volume.

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Section II will discuss both HBT and HEMT device technologies. The MMIC's and module designs, as well as HBT and HEMT device modeling, will be discussed in Section III. The individual MMIC chips and module measurement results are illustrated in Section IV and followed by a brief summary.

II. Device Technology Selection

The three MMIC chips are all developed using GaAs-based device technologies. The 23.5 GHz VCO design is based on HBT devices mainly owing to its superior $1/f$ noise. A 2-μm self-aligned base ohmic metal (SABM) HBT process on 3-in.-diameter GaAs substrate was selected as the baseline HBT process in TRW production line. The $2 \times 10\ \mu m^2$ quad emitter HBT device used in the VCO has a typical unit current gain frequency (f_T) of 22 GHz and maximum oscillation frequency ($f_{\max}$) of 40 GHz. The HBT device process and characteristics were documented in [5]–[7].

The 23.5–94 GHz frequency quadrupler used 0.1-μm pseudomorphic (PM) low noise AlGaAs/InGaAs HEMT's while the three-stage output amplifier utilized 0.1-μm PM power AlGaAs/InGaAs HEMT's. The low noise HEMT was optimized for high gain operation at W-band. The 22% PM InGaAs HEMT uses planar doping to achieve high channel aspect ratio as well as higher electron transfer efficiency. The HEMT device structure and MMIC fabrication process used for this work has been previously reported [8]–[9]. The power HEMT differs from the low noise HEMT by the introduction of an additional planar doping in the channel region to increase the device current handling capability. This also improves the transconductance linearity over a wider range of gate voltages. Since the AlGaAs layer is undoped, the Schottky gate recessed to this undoped region has a high Schottky gate-drain breakdown. The power HEMT device structure and MMIC fabrication process used here were reported [1], [10], [11].

Both the HEMT devices were passivated with Si_3N_4 layer by plasma-enhanced chemical vapor deposition to enhance device reliability in the production [12]. The passivated device with a 40-μm total gate-width (four gate-fingers) typically shows a dc transconductance (G_m) of 600 mS/mm and an f_T of higher than 100 GHz.

III. MMIC's and W-Band Source Module Design

The MMIC's used in the W-band source module are all designed using microstrip lines on a 100-μm-thick GaAs substrate. Extensive circuit simulations were performed during the design phase, including small signal linear simulations and large signal nonlinear simulations using the harmonic balanced

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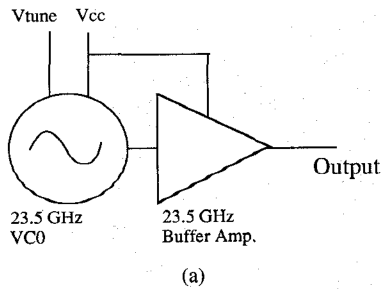

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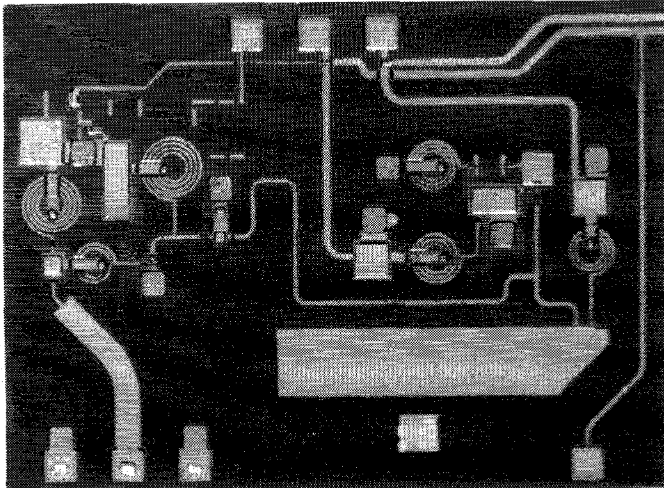

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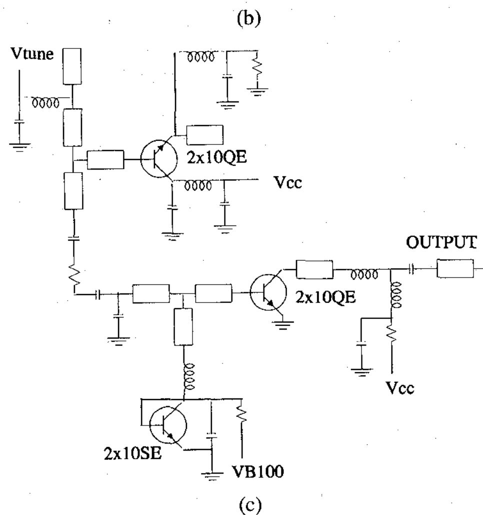


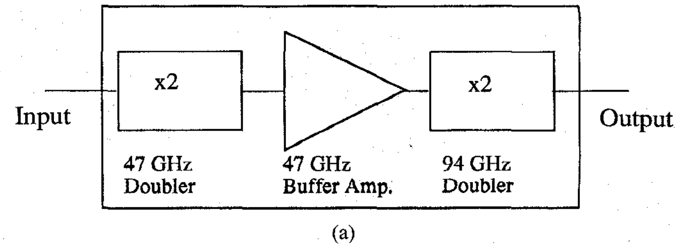
(c)

Fig. 1. The (a) functional block diagram, (b) chip photograph of the 23.5 GHz HBT VCO, and (c) schematic diagram of the 23.5 GHz HBT VCO plus buffer amplifier.

technique. The linear small signal equivalent circuit model parameters of the devices were obtained from the measured small signal S-parameters up to 50 GHz using curve fit technique. The resulting parameters are consistent with the estimated values based on device physical dimensions and parameters. The Curtice-Ettenberg FET asymmetric model and Gummel-Poon spice model were used to describe the nonlinear behavior of HEMT and HBT devices, respectively. The individual MMIC and the module designs are described below.

A. 23.5 GHz VCO

The 23.5 GHz HBT MMIC VCO circuit developed in this work encompassed both a common collector bias tuned VCO



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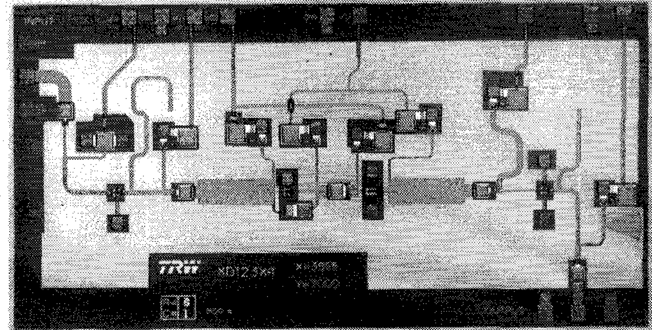


(b)

Fig. 2. The (a) block diagram and (b) chip photograph of the 23.5–94 GHz frequency quadrupler.

and a buffer amplifier. The functional block diagram and chip photograph of the MMIC is shown in Fig. 1(a) and (b). The VCO circuit utilizes a 2×10 μm^2 emitter HBT device with an RF grounded collector biased from +5 V, the VCO schematic diagram is shown in Fig. 1(c). A small capacitive stub is connected to the emitter to make the oscillating device unstable. The emitter bias is grounded through an emitter resistor that is key to setting the tuning voltage range and improving the phase noise. The dc resistor provides bias stabilizing feedback to help prevent low frequency device noise from modulating the bias point and therefore the oscillation frequency. The main frequency determining resonator is connected to the base of the oscillator transistor. The resonator consists of a fully monolithic high impedance inductive section followed by a low impedance open circuit resonator of approximately quarter wave length. The low impedance resonator significantly improves the stability of the oscillator. Its electrical length serves to greatly increase the reactance slope parameter of the resonator [16], and therefore the Q of the finished oscillator.

The output of the oscillator is inductively tapped off the high impedance resonator with a high impedance quarter wave structure design to transform the 50 Ω input impedance of the buffer amplifier up to a high impedance. This allows for a very lightly coupled load so that the energy lost to the output does not significantly degrade phase noise. The oscillator is tuned by changing the base voltage on the oscillator device. The bias tuned approach was chosen to eliminate the need for a series variable capacitance tuning element. Realization of such an element on chip would have added significant losses to the resonator circuit. Using an off chip tuning element was not an option due to added manufacturing cost and complexity.

A buffer amplifier was added to increase the output power and isolate the VCO from frequency pulling effects of the load. The oscillator output power variations caused by changing

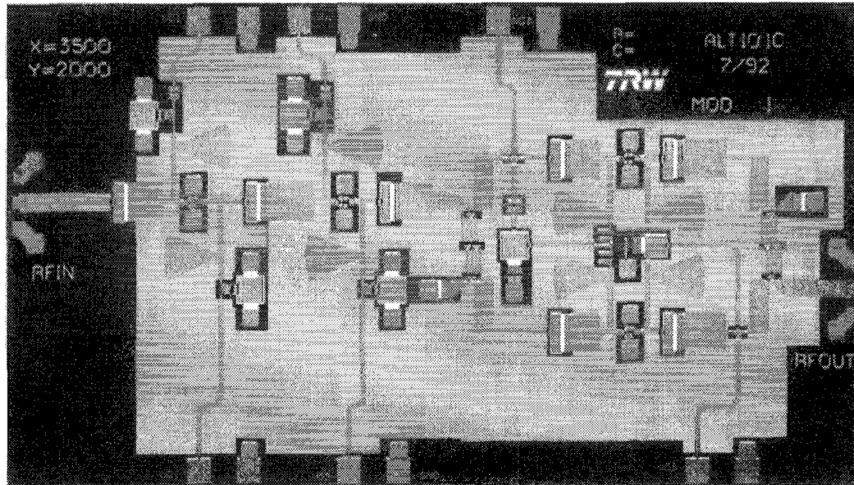


Fig. 3. The chip photograph of W-band output amplifier.

the bias of the oscillator transistor were reduced by partially saturating the output amplifier. The amplifier is a single ended design based on the same size device as the oscillator. The bias of the amplifier transistor was stabilized with a simple current mirror.

Both linear simulation in the frequency domain and nonlinear simulation were performed in designing the VCO circuit. The simulation of the VCO started with linear small signal modeling to get the VCO close to frequency. The nonlinear simulation using harmonic balanced technique was performed to confirm both the oscillation frequency and output power. The simulation agree well with the measured results.

B. 23.5–94 GHz Frequency Quadrupler

Fig. 2 shows the block diagram and chip photograph of the 23.5–94 GHz frequency quadrupler, which consists of a 23.5–47 GHz frequency doubler, a 47-GHz buffer amplifier, and a 47–94 GHz frequency doubler [17]. The 47–94 GHz frequency doubler utilizes a four-finger 80 μm HEMT device. The design follows a conventional single-ended common source configuration design procedure described in [9]. An open stub providing an RF short at the fundamental frequency is employed in output matching network to suppress the fundamental signal. The HEMT device operates near its pinch-off condition in order to obtain optimal nonlinearity for maximum output power of the second harmonic signal, thus good dc to RF conversion efficiency can be achieved. The 23.5–47 GHz frequency doubler also uses a four-finger 80-μm device. The design is similar to the 47–94 GHz doubler mentioned above.

The 47-GHz buffer amplifier is a single-ended two-stage design with resistive feed back at first stage for stability consideration. A four-finger 80-μm device is used in the first stage to drive a four-finger 160-μm device in the second stage. All matching networks consist of series and shunt microstrip lines. Silicon nitride metal-insulator-metal (MIM) capacitors are used for RF by-pass and dc blocking. Gate and drain bias lines of each stage are connected together, respectively, for ease of biasing the two-stage amplifier.

Both frequency doublers and the buffer amplifier cascading using 50-Ω transmission lines form the frequency quadrupler. MIM capacitors were used for dc blocking. The complete 23.5–94 GHz frequency quadrupler has a chip size of 4 $\times$ 2 mm^2.

There are some design issues for the present MMW frequency doubler design. Since the HEMT device operates near its pinch-off condition with a large signal input, the predicted dc-IV curves via nonlinear model must be able to represent the actual HEMT device behavior from pinch-off to peak transconductance. Unfortunately, the Curtice-Ettenberg FET model usually can model the peak transconductance region well but not the pinch-off region. Also, the harmonic balance technique requires several higher order harmonics in the circuit analysis. Those frequencies can be way above 100 or 200 GHz for which most models become questionable. All these factors will affect the simulation accuracy. For this design, the measured results deviated from the simulated frequency response by 3 GHz.

C. 94-GHz Three-Stage Output Amplifier

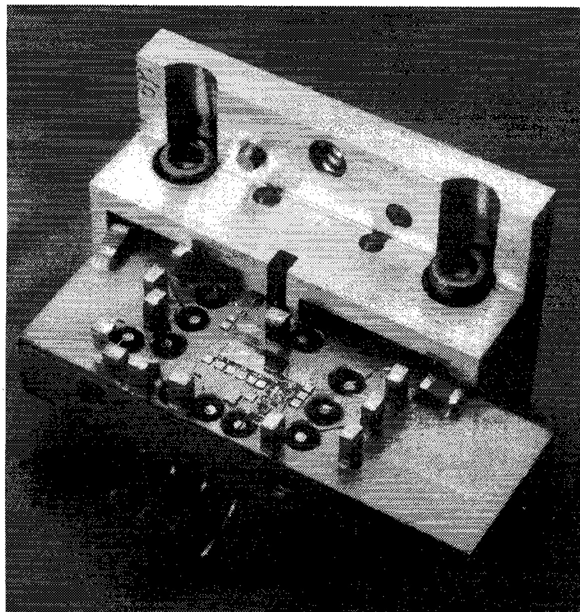
The three-stage output amplifier is a two-stage single-ended amplifier cascaded with a single-stage balanced output amplifier. The chip photograph is shown in Fig. 3. Each stage utilizes a 40-μm HEMT with four gate fingers. The output amplifier design follows the design/analysis methodology reported in [14]. The chip size is 3.5 $\times$ 2 mm^2.

D. W-Band Source Module

The W-band source module was assembled in a WR10 waveguide test fixture as shown in Fig. 4. Ribbon bonds were used to connect the VCO-quadrupler and quadrupler-amplifier interfaces. Anti-podal finline transition on 125-μm-thick fused silica substrate was used to couple the signal from microstrip line of the output amplifier to the waveguide.

IV. Measurement Results

All three MMIC chips used in the W-band source module were tested separately before being assembled in the module.



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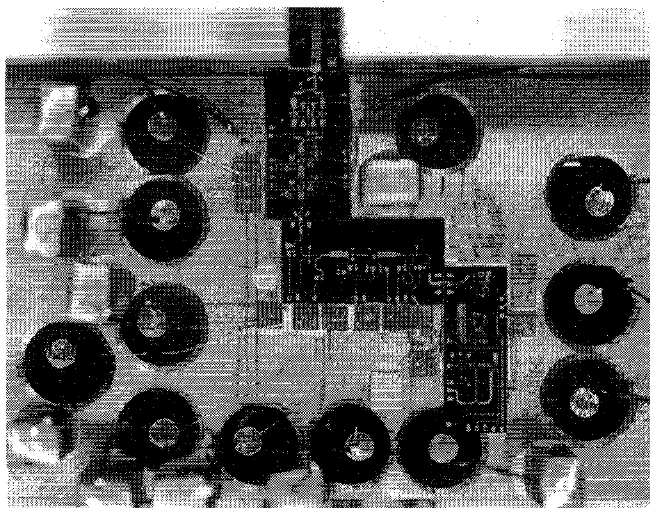

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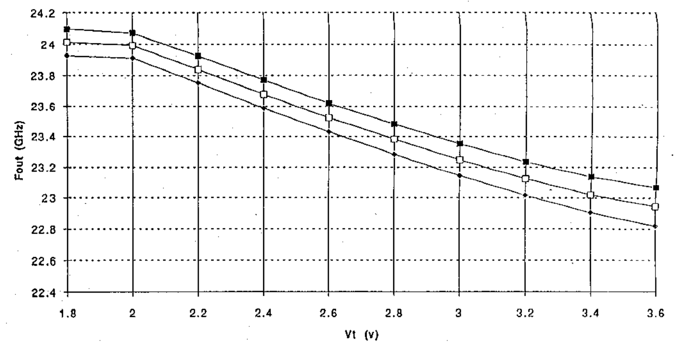
Fig. 4. The photographs of the W-band source module. (a) The complete unit. (b) A closer view of three MMIC chips in the module.



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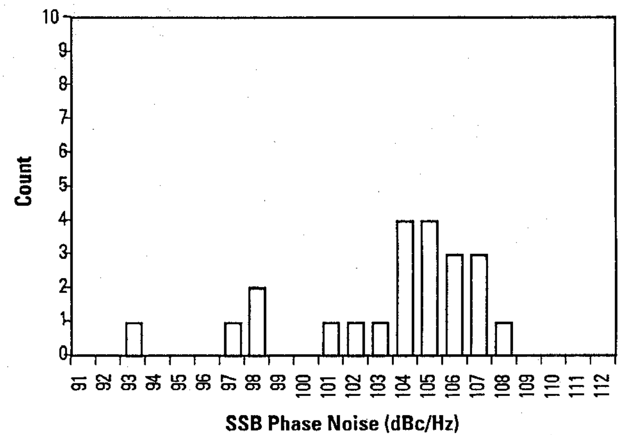


(b)

Fig. 5. (a) The average output frequency and $\pm$ one standard deviation as function of tuning voltage of the K-band HBT VCO. (b) Histogram of single side band phase noise (dBc/Hz at 1 MHz offset) for the VCO plus buffer amplified chip measurement taken across an entire wafer.

The 23.5-GHz VCO was tested via on-wafer probing for an entire wafer. The average output frequency and $\pm$ one standard deviation as function of tuning voltage are plotted in Fig. 5(a). It exhibits an average tuning bandwidth of greater than 1 GHz from 23–24 GHz for the tuning voltage of 1.8–3.6 V. The output power varies from 3 to 5 dBm. The histogram of single side band phase noise for the VCO plus buffer amplifier chip measurements taken across an entire wafer are shown in Fig. 5(b). The measurements show an average phase noise at 1-MHz offset of -104 dBc/Hz. This corresponds to an approximate phase noise of -79 dBc/Hz at 100-kHz offset. The phase noise at 100-kHz offset from this work is shown summarized with other phase noise results obtained at TRW and from literature, as shown in Fig. 6. It is noticed that this phase noise comparison chart summarizes microstrip resonator oscillators only. Each set of data points represent the tuning range of the individual oscillator circuits at the phase noise level measured. This work falls approximately in line with other previous HBT oscillators developed. The oscillator circuits were also measured over temperature. The free running oscillator exhibited a temperature drift of -2.9 MHz/°C with less than 1 dB change in phase noise over the -30°C to $+60$°C temperature range.

Some micro-cells of the 23.5–94 GHz frequency quadrupler were evaluated first before the complete quadrupler testing. The 23.5–47 GHz frequency doubler and the 47-GHz buffer amplifier were measured using on-wafer probing technique. The 23.5–47 GHz frequency doubler exhibits a measured conversion loss of 5–6 dB for the input power of 5 dBm from 23.5–25 GHz as shown in Fig. 7, while the 47-GHz buffer amplifier has a measured small signal gain of 8 dB. The complete 23.5–94 GHz frequency quadrupler was then measured in a test-fixture with the input port a coaxial cable connector transition to microstrip line, and the output port a finline transition on 125-μm-thick fused silica substrate from microstrip line to WR10 waveguide. Fig. 8 shows the measured output power versus input power of the frequency quadrupler at three different frequencies. A conversion loss of 5 dB was obtained at an input power of 2 dBm at 24.5 GHz. During the test, the HEMT devices in the doublers were biased at 2-V drain voltages with gate biased near pinch-off region.

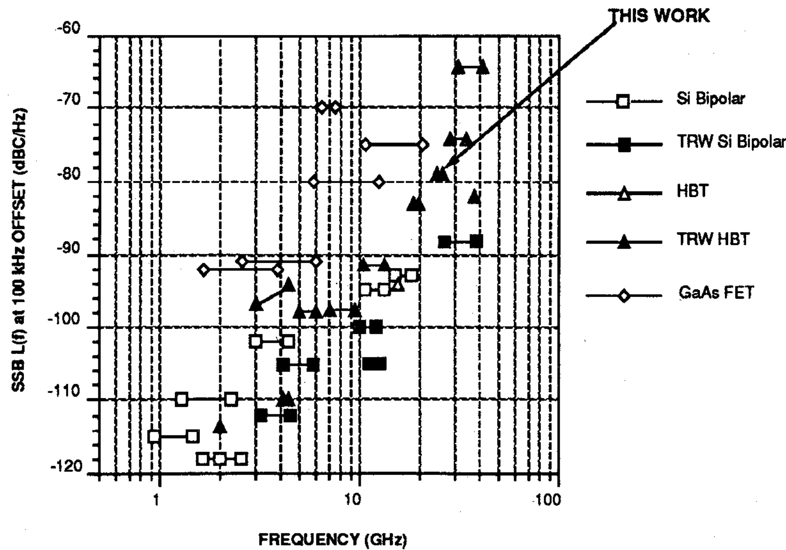


Fig. 6. Summary chart of the phase noise at 100-kHz offset from this work with other phase noise results obtained at TRW and from literature.

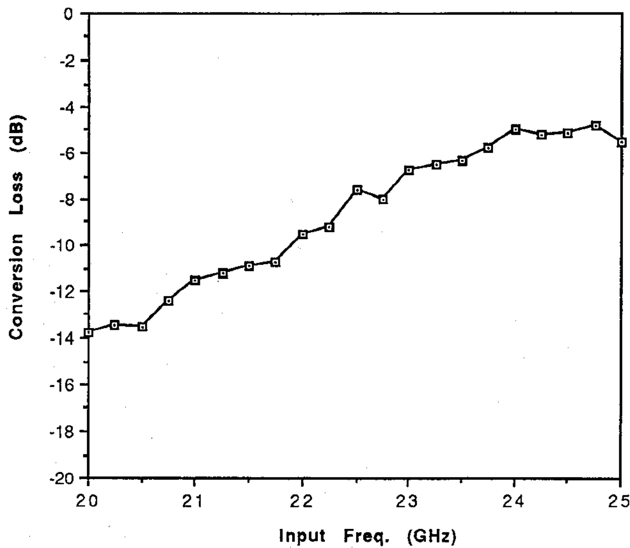


Fig. 7. The conversion loss versus input frequency for the 23.5–47 GHz-doubler.

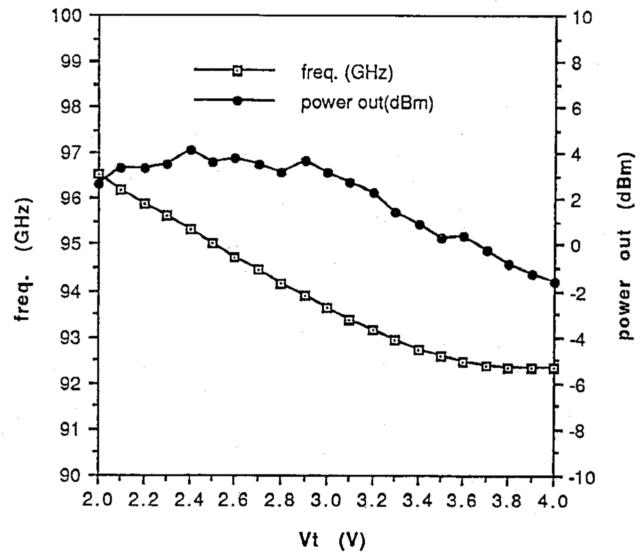


Fig. 9. The output power and tuning frequency versus tuning voltage of thecomplete W-band source module.

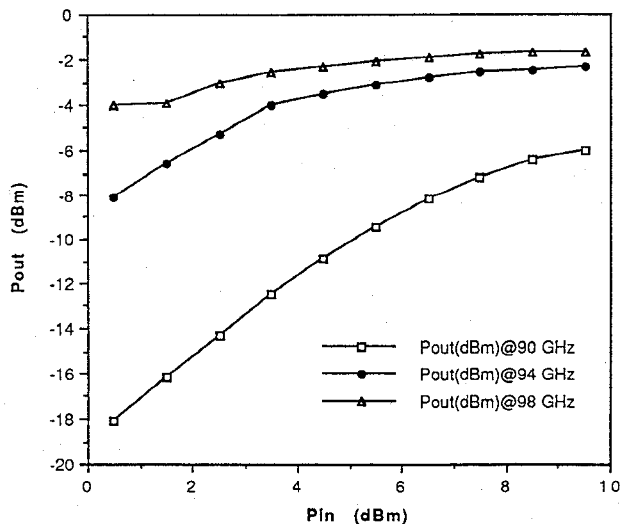
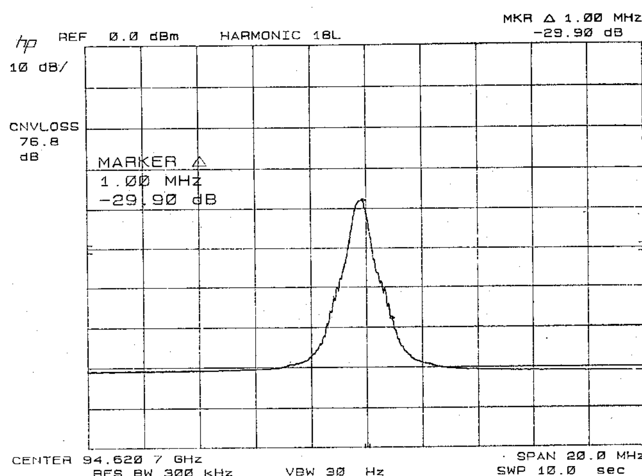


Fig. 8. The output power versus input power at three different frequencies for the monolithic frequency quadrupler.

The three-stage W-band output amplifier was measured on a verified W-band on-wafer probe test set [15]. It showed a typical linear gain of 10–12 dB and an output power of 14 dBm at 94 GHz.

The complete W-band source module, shown in Fig. 4, demonstrated a tuning band-width of 4 GHz (92.5–96.5 GHz) and a peak output power of 3 dBm at 94–95 GHz. The output power and frequency as functions of tuning voltage are plotted in Fig. 9. The 3-dB tuning bandwidth is greater than 3 GHz. The measured frequency spectrum centered at 94.6 GHz of the module was plotted in Fig. 10(a). The phase noise was evaluated via a single-oscillator phase-noise measurement technique using a delay line as an FM discriminator [18]–[19]. The phase noise of dBc/Hz as a function of offset frequency away from center frequency is plotted in Fig. 10(b). It shows −92 dBc/Hz at 1-MHz offset and −80 dBc/Hz at 100-kHz offset. By adding 6 dB/octave to the phase noise measurement



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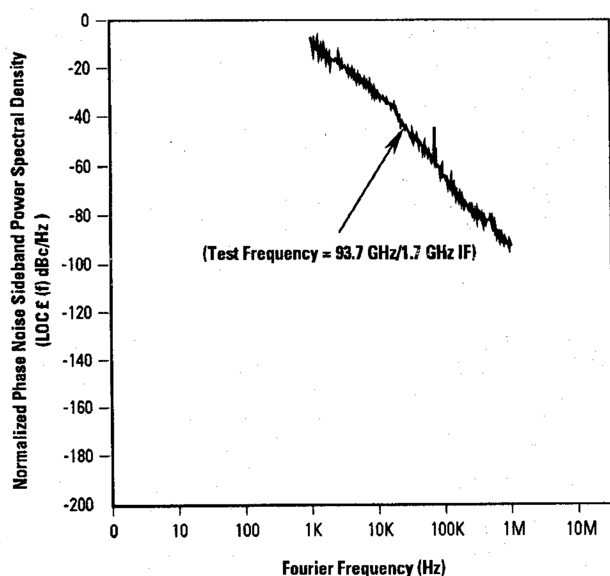

(b)

Fig. 10. (a) The spectrum analyzer plot of the W-band source module. (b) Phase noise of the W-band source module evaluated via a single-oscillator phase-noise measurement technique using a delay line as an FM discriminator. The phase noise of dBc/Hz is plotted as a function of the offset frequency away from center frequency.

of 23.5 GHz VCO, -104 dBc/Hz, to estimate the phase noise of the frequency-quadrupled W-band source, one can obtain -92 dBc/Hz at 1-MHz offset, which is consistent with the phase noise measurement result.

V. Summary

We have demonstrated the W-band source module providing 4-GHz tuning bandwidth (92.5–96.5 GHz) with peak output power of 3 dBm at 94–95 GHz and good phase noise. This module utilized three MMIC chips fabricated in TRW production lines, which can easily be obtained in volume. Design of the MMIC chips and complete measurement data were discussed in detail. The design simplicity and good performance of this source module will make it suitable for many W-band system applications.

Acknowledgment

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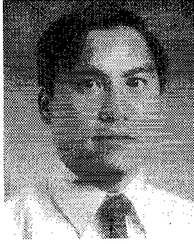

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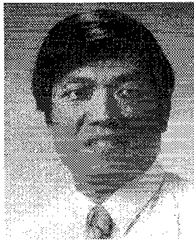

G. Samuel Dow (S'78-M'82) was born in Tainan, Taiwan, on April 12, 1954. He received the diploma in electrical engineering from Taipei Institute of Technology, Taipei, Taiwan, in 1974 and the M.S.E.E. degree from University of Colorado, Boulder, in 1981.

From 1981–1983 he was with Microwave Semiconductor Corporation, where he was responsible for the first demonstration of 0.5 W output power at 20 GHz with the GaAs MESFET technology. From 1984–1987, he was a staff engineer with Hughes Aircraft Company, Microwave Products Division, where he engaged in the modeling and characterization of MESFET power devices, design of wideband and high efficiency power amplifiers and millimeter-wave receiver components. He joined TRW in 1987. He is currently Section Head of EHF/RF MMIC section and Subproject Manager of MMIC Design of the ARPA MIMIC program. His research interests at TRW have included microwave and millimeter-wave IC design with HEMT and HBT millimeter-wave systems and applications. During the past several years, his group has published very extensively in the area of microwave and millimeter-wave monolithic circuit design up to 120 GHz.

Kin L. Tan (M'90) received the B.S.E.E. and M.S.E.E. degrees from Purdue University in 1983 and 1985, respectively.

After graduating from Purdue University, he held a research scientist position at Honeywell Physical Sciences Center where he worked on submicron digital GaAs MESFET's for high speed SRAM, A/D converters, and signal processors. In 1988, he joined Hughes Microwave Products Division where he was involved in the development of GaAs microwave MESFET's, HEMT's and HBT's. Since 1989, he has been with TRW Electronic Systems and Technology Division where he was responsible for developing state-of-the-art GaAs and InP-based HEMT's and the transfer to production of III–V millimeterwave HEMT MMIC's. He is currently the assistant program manager for GaAs Manufacturing on the ARPA funded MIMIC Phase II program. He has published and presented over 60 papers in the areas of III–V compound semiconductor devices, IC's and processing.

Mr. Tan is a two-time receipient of TRW Chairman's Award for Innovation for his contributions to millimeter wave HEMT's and flexible GaAs manufacturing line.

Aaron K. Oki (M'85) was born in Honolulu, HI. He received the B.S. degree in electrical engineering in 1983 from the University of Hawaii, Manoa, and the M.S. degree in electrical engineering and computer science in 1985 from the University of California, Berkeley.

Since joining TRW as a member of technical staff in 1985 he has been working on production and advanced development of HBT technology. In 1990 he became the principle investigator for HBT IR&D and section head of the HBT products section.

Barry R. Allen (S'82, M'83) was born in Cadiz, KY, on November 5, 1947. He received the B.S. degree in Physics and the M.S. and Sc.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, in 1976, 1979, and 1984, respectively.

He joined TRW in 1983 as a senior staff member and has held a number of positions since then. Science 1983 he has been involved in all aspects of MMIC design and modeling. His main interests are low noise receiving systems, millimeter wave circuits, and accurate circuit modeling. From 1970–1975, he was with the Chesapeake and Potomac Telephone Company of Virginia, supporting microwave and radio telecommunications systems. From 1975–1983, he was a member of the Research Laboratory of Electronics at MIT, both as an undergraduate and as a research assistant in radio astronomy. While at MIT, he was responsible for the development of room temperature and cryogenic low noise receiving systems spanning 300 MHz –43 GHz. He is currently a senior scientist in the Electronic Systems and Technology Division. His present assignment is assistant program manager for design and advanced technology on the ARPA funded MIMIC Phase 2 Program. He has published several papers on circuit applications of heterostructure devices and MMIC's.

In 1991, Dr. Allen became a TRW Technical Fellow in the Space and Defense Sector for contributions to the application and manufacturing of GaAs MMIC's. He was awarded TRW's Chairman's Award for Innovation in 1992 and 1993.